

IN THE DRAWINGS:

Enclosed herein are replacement formal drawings of Figures 1, 11 and 12, which include corrections to and are submitted as replacements for the originally filed drawings.

REMARKS

The above amendments and the following remarks are fully and completely responsive to the Office Action dated May 18, 2005. Claims 1-18 are pending in this application. By this Amendment, claims 1, 6 and 14 have been amended and Figs. 1, 11 and 12 replaced. In the outstanding Office Action, the drawings were objected to and claims 1-18 were rejected under 35 U.S.C. § 103(a) (three different rejections). No new matter has been added. Claims 1-18 are presented for reconsideration.

Specification Amendment

The specification has been amended so that the specification is consistent with the amendments to Figs. 1, 11 and 12.

Drawing Objection

The Office Action objected to the drawings as failing to show every feature of the invention specified in the claims. Applicants have amended and replaced Figs. 1, 11 and 12 so that the drawings now show every feature recited in the claims. Therefore, Applicants request reconsideration and withdrawal of the objection to the drawings.

35 U.S.C. § 103(a)

Claims 1-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sim et al. (U.S. Patent No. 6,546,511, "Sim") in view of Brauch et al. (U.S. Patent No. 6,550,023, "Brauch"). In making this rejection, the Office Action asserts that the combination of these two references teaches and/or suggests each element of the claimed invention. The Office Action also asserts that one of ordinary skill in the art

would combine these two references. Applicants disagree and request reconsideration of this rejection.

Claim 1, as amended, recites in part:

comparing plural pieces of read data read from the plurality of memory circuits in a read operation with one another and generating a first signal as first comparison results;

comparing one of the plural pieces of read data, which is read from a predetermined one memory circuit, with write data and generating a second signal as a second comparison result in parallel with the first signal; and

testing the plurality of memory circuits based on the first and second signals.

Sim discloses comparing a plurality of output signals output from the plurality of function blocks with one another and comparing the selected one of the output signals with the target value when the output signals are at the same level.

However, neither Sim nor Brauch discloses generating in parallel a first signal (decision signal K2) as comparison results of plural pieces of read data and a second signal (confirmation signal K1) as a comparison result of one of the plural pieces of read data and write data.

Consequently, Applicants could find no disclosure “comparing one of the plural pieces of read data, which is read from a predetermined memory circuit, with write data and generating a second signal as a second comparison result in parallel with the first signal”.

Consequently, the combination of Sim and Brauch fails to teach and/or suggest the claimed invention. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-5 under 35 U.S.C. § 103(a).

Claims 6-8, 10 and 14-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sim in view of Usui et al. (U.S. Patent No. 5,793,774, "Usui"). In making this rejection, the Office Action asserts that the combination of these two references teaches and/or suggests the claimed invention. The Office Action also asserts that the combination of these two references would be obvious to one of ordinary skill in the art.

Claims 9, 11-13 and 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sim in view of Usui as applied to claims 6 and 14 above, and further in view of Tomari (U.S. Patent No. 6,480,979). In making this rejection, the Office Action asserts that the combination of these three references teaches and/or suggests the claimed invention. The Office Action also asserts that one of ordinary skill in the art would combine these three references. Applicants disagree and request reconsideration of this rejection.

Claim 6, as amended, recites in part:

a comparator coupled to the plurality of memory circuits for comparing plural pieces of read data respectively read from the plurality of memory circuits with one another in the test mode and generating a first signal as first comparison results, wherein in the test mode, the processing unit compares data written in the plurality of memory circuits with one of the plural pieces of read data read from the predetermined one memory circuit and supplied from the multiplexer and generates a second signal as a second comparison result to test the plurality of memory circuits based on the first and second signals, wherein the comparator generates the second signal in parallel with the first signal.

Claim 14, as amended, recites in part:

a comparator for receiving plural pieces of read data read from the plurality of memory circuits and comparing the plural pieces of read data with one another to generate a first signal as first comparison results; and

a processing unit for comparing one of the plural pieces of read data, which is read from a predetermined memory circuit, with write data and generating a second signal as a second comparison result to test the plurality of memory circuits based on the first and second signals, wherein the processing unit generates the second signal in parallel with the first signal.

Usui discloses the control means 101 as a bus master, the memory controlling means 102 for performing a chip selection, the command sequence detecting means 107, the selecting means 108 for selecting one of the paths (Fig. 4), and the comparator means 111 for comparing error check codes (Fig. 8).

However, Usui does not disclose a comparator for comparing read data and write data. Additionally, neither Sim nor Usui discloses generating the first signal and the second signal in parallel with each other.

Applicants have carefully reviewed Sim, Usui and Tomari. These three references, either alone or in combination, fail to teach and/or suggest the above claim elements.

Regarding claim 6, these references fail to teach and/or suggest that the comparator generates the second signal in parallel with the first signal.

Regarding claim 14, the combination of these three references fails to teach and/or suggest that the processing unit generates the second signal in parallel with the first signal.

Accordingly, the combination of Sim, Usui and Tomari fails to teach and/or suggest the claimed invention. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 6-18 under 35 U.S.C. § 103(a) (two different rejections).

Conclusion

Applicants' amendments and remarks have overcome the objection and rejections set forth in the Office Action dated May 18, 2005. Specifically, Applicants' amendment to Figs. 1, 11 and 12 overcomes the objection to the drawings. Applicants' remarks have distinguished claims 1-5 from the combination of Sim and Brauch and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Applicants' remarks have also distinguished claims 6-8, 10 and 14-15 from the combination of Sim and Usui and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Applicants' remarks have also distinguished claims 9, 11-13 and 16-18 from the combination of Sim, Usui and Tomari and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Accordingly, claims 1-18 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1-18.

Applicants submit that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 108075-00072.

Respectfully submitted,
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Enclosures: Replacement Sheets Figs. 1, 11 and 12
Request for Continued Examination